PTN3393

2-lane DisplayPort to VGA adapter test IC

Rev. 2 — 27 July 2012 **Objective product brief**

1. General description

The PTN3393 is a DisplayPort to VGA adapter IC designed to connect a DisplayPort source to a VGA sink. The PTN3393 integrates a DisplayPort receiver and a high-speed triple video digital-to-analog converter that supports display resolutions from VGA to WUXGA. The PTN3393 supports either one or two DisplayPort v1.1a lanes operating at either 2.7 Gbit/s or 1.62 Gbit/s per lane. The PTN3393 supports 'Flash-over-AUX' capability enabling simple firmware upgradability in the field.

The PTN3393 supports I^2C-bus over AUX per DisplayPort v1.1a specification, and bridges the VESA DDC channel to the DisplayPort Interface.

The PTN3393 is designed for single supply and minimizes application costs. It can be powered directly from the DisplayPort source side 3.3 V supply without a need for additional core voltage regulator. The VGA output is powered down when there is no valid DisplayPort source data being transmitted. The PTN3393 also aids in monitor detection by performing load sensing and reporting sink connection status to the source.

2. Functional diagram

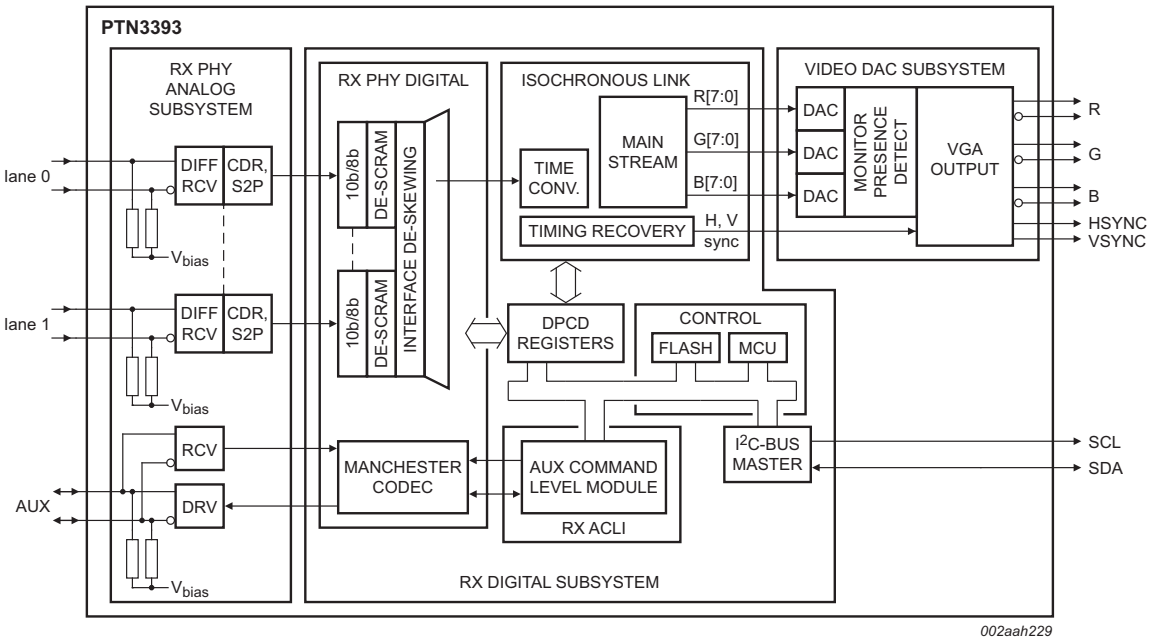


Fig 1. Functional diagram of PTN3393

3. Pinning information

3.1 Pinning

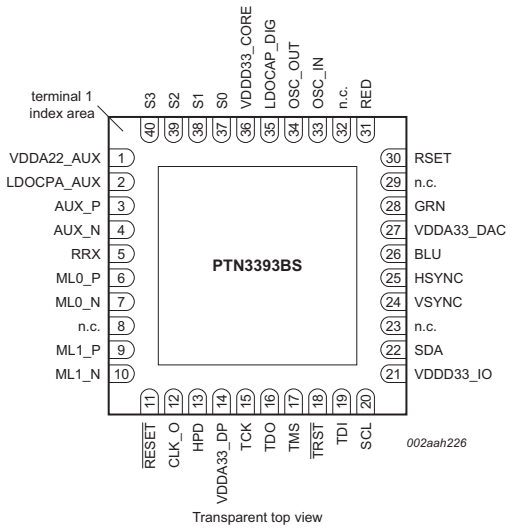


Fig 2. Pin configuration for HVQFN40

3.2 Pin description

Table 1. Pin description

Symbol	Pin	Type	Description
Power			
VDDD33_CORE	36	power	Digital core 3.3 V supply voltage
VDDA33_AUX	1	power	Analog AUX, bias and PLL 3.3 V supply voltage
VDDA33_DP	14	power	Analog 3.3 V supply for DisplayPort receiver module
VDDD33_IO	21	power	I/O 3.3 V supply voltage
VDDA33_DAC	27	power	Analog 3.3 V supply for DAC
LDOCAP_AUX	2	power	1.8 V AUX supply decoupling
LDOCAP_DIG	35	power	1.8 V digital core supply decoupling
DisplayPort			
ML0_P	6	self-biasing differential input	DisplayPort main lane signal lane 0, positive
ML0_N	7	self-biasing differential input	DisplayPort main lane signal lane 0, negative
ML1_P	9	self-biasing differential input	DisplayPort main lane signal lane 1, positive
ML1_N	10	self-biasing differential input	DisplayPort main lane signal lane 1, negative
AUX_P	3	self-biasing differential input/output	DisplayPort auxiliary channel signal, positive
AUX_N	4	self-biasing differential input/output	DisplayPort auxiliary channel signal, negative

Table 1. Pin description *…continued*

Symbol	Pin	Type	Description
HPD	13	3.3 V TTL single-ended output	Hot Plug Detect
RGB DAC outputs			
BLU	26	analog output	'blue' current analog output
GRN	28	analog output	'green' current analog output
RED	31	analog output	'red' current analog output
RSET	30	analog input/output	DAC full-scale current control resistor. Pull down to ground by an external 1.2 kΩ ± 1 % resistor.
DDC			
SCL	20	single-ended 5 V open-drain DDC I/O	5 V sink-side DDC clock I/O. Pulled up by external resistor to 5 V.
SDA	22	single-ended 5 V open-drain DDC I/O	5 V sink-side DDC data I/O. Pulled up by external resistor to 5 V.
Monitor-side sync			
HSYNC	25	single-ended 3.3 V TTL output	horizontal sync signal to monitor
VSYNC	24	single-ended 3.3 V TTL output	vertical sync signal to monitor
JTAG			
TCK	15	input	JTAG clock input
TDO	16	output	JTAG data output
TMS	17	input	JTAG mode select input
$\overline{\text{TRST}}$	18	input	JTAG reset (active LOW) input
TDI	19	input	JTAG data input
Miscellaneous			
S0	37	input	Open (internal pull-down) = logic 0 Implement VGA-side monitor detect according to *VESA DisplayPort Standard v1.1a*, sections 7 and 8. HIGH (external pull-up) = logic 1 Set HPD HIGH upon VGA monitor detection; set HPD LOW upon VGA monitor detachment.
S1	38	input	reserved; leave open-circuit (default internal pull-down)
S2	39	input	Open (internal pull-down) = logic 0 to set default I^2C-bus speed to 50 kbit/s. HIGH (external pull-up) = logic 1, to set default I^2C-bus speed to 10 kbit/s. This pin may be left open-circuit (internal pull-down) or tied to V_{DD} according to the desired default I^2C-bus speed. See more explanation about S2 pin setting and DPCD register 00109h.
S3	40	input	reserved; leave open-circuit (default internal pull-down)
$\overline{\text{RESET}}$	11	input	Hardware reset input (active LOW); internal pull-up. A capacitor must be connected between this pin and ground. A 1 µF capacitor is recommended.
CLK_O	12	output	DisplayPort receiver test clock output
OSC_IN	33	input	crystal oscillator input

Table 1. Pin description *...continued*

Symbol	Pin	Type	Description
OSC_OUT	34	output	crystal oscillator output
RRX	5	input	Receiver termination resistance control. A 12 kΩ resistor must be connected between this pin and LDOCAP_AUX (pin 2).
n.c.	8, 23, 29, 32	-	not connected

4. Display resolution

Table 2 lists some example display resolutions and clock rates that PTN3393 supports.

Table 2. Display resolution and pixel clock rate

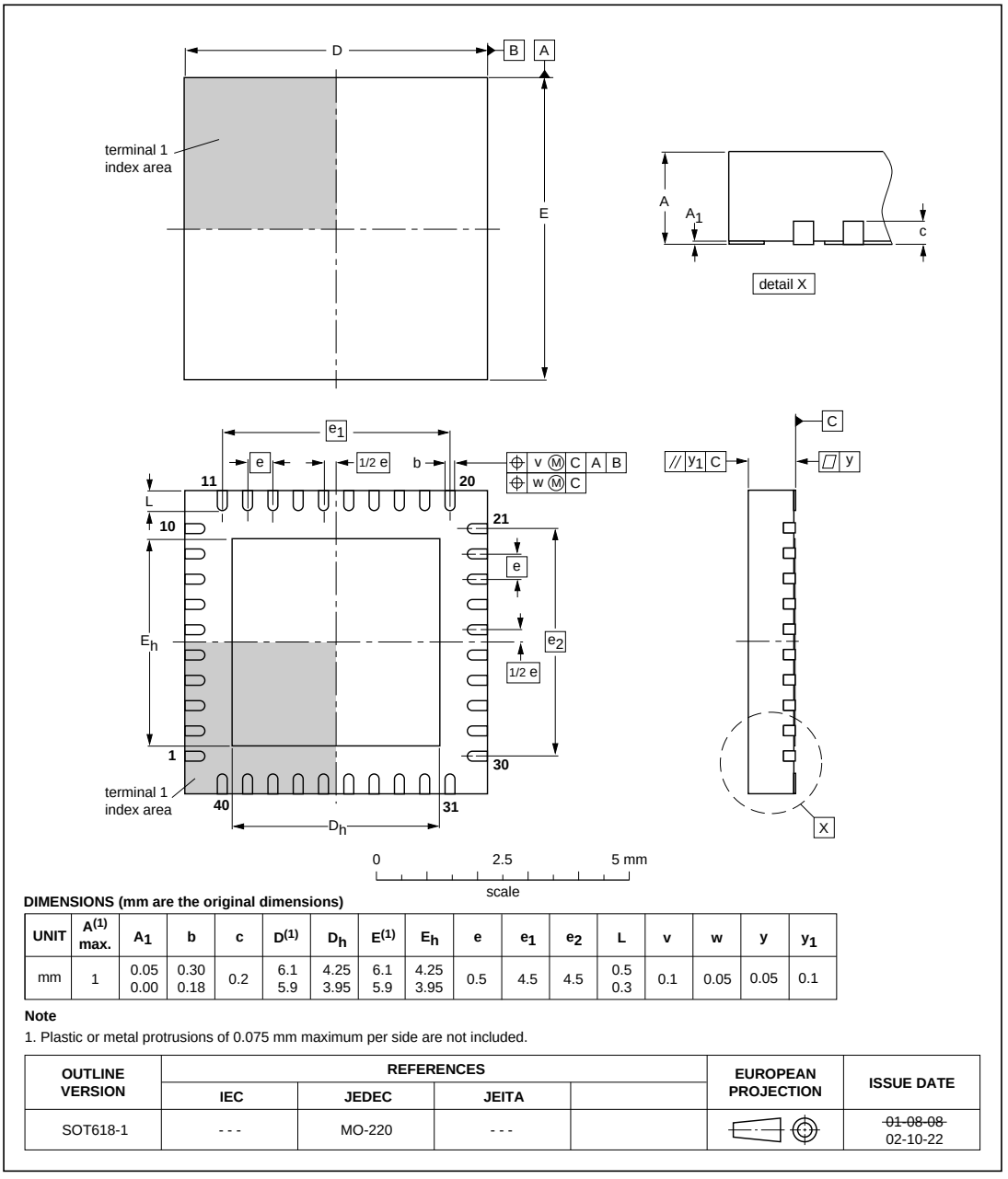
Display type	Active video		Total frame		Bits per pixel	Frame rate (Hz)	Pixel clock (MHz)	Data rate (Gbit/s)
	Horizontal	Vertical	Horizontal	Vertical				
VGA	640	480	800	525	24	59.94	25.175	0.8
SVGA	800	600	1056	628	24	60.32	40.002	1.2
XGA	1024	768	1344	806	24	60	64.996	1.9
XGA+	1152	864	1520	806	24	60	81.806	2.45
WXGA	1280	768	1664	897	24	60	79.672	2.39
WXGA+	1400	900	1848	934	24	60	103.562	3.11
XGA+	1152	864	1520	806	24	60	81.806	2.45
	1366	768	1792	798	24	60	85.801	2.57
SXGA	1280	1024	1688	1066	24	60.02	108.000	3.2
SXGA	1280	1024	1728	1072	24	85	157.455	4.72
SXGA+	1400	1050	1864	1089	24	60	121.794	3.65
	1600	900	2112	934	24	60	118.356	3.55
WSXGA+	1680	1050	2240	1089	24	60	146.362	4.39
UXGA	1600	1200	2160	1250	24	60	162.000	3.9
UXGA	1600	1200	1760	1243	24	75	164.076	4.92
UXGA	1600	1200	2160	1250	18	85	229.500	5.16
FHD	1920	1080	2200	1125	24	60	148.500	4.46
WUXGA	1920	1200	2592	1245	18	59.885	193.251	4.35
WUXGA	1920	1200	2080	1235	24	59.95	154.000	4.62
QXGA	2048	1536	2144	1555	24	49.266	164.249	4.9
QWXGA	2048	1152	2720	1188	24	49.979	161.500	4.84
QWXGA	2048	1152	2208	1185	24	59.909	156.751	4.7

The available bandwidth over a 2-lane HBR DisplayPort 1.1a link limits pixel clock rate support to:

- 240 MHz at 6 bpc
- 180 MHz at 8 bpc

5. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.5	4.5	4.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT618-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 3. Package outline SOT618-1 (HVQFN40)

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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