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Kind regards,

Team Nexperia

# DATA SHEET

## **PDTA123E series**

**PNP resistor-equipped transistors;**

**R1 = 2.2 k $\Omega$ , R2 = 2.2 k $\Omega$**

Product data sheet  
Supersedes data of 2004 Apr 07

2004 Aug 02

## PNP resistor-equipped transistors; R1 = 2.2 k $\Omega$ , R2 = 2.2 k $\Omega$

## PDTA123E series

### FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

### APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	–	–50	V
I <sub>O</sub>	output current (DC)	–	–100	mA
R1	bias resistor	2.2	–	k $\Omega$
R2	bias resistor	2.2	–	k $\Omega$

### DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

### PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA123EE	SOT416	SC-75	5C	PDTC123EE
PDTA123EEF	SOT490	SC-89	6C	PDTC123EEF
PDTA123EK	SOT346	SC-59	42	PDTC123EK
PDTA123EM	SOT883	SC-101	F7	PDTC123EM
PDTA123ES	SOT54 (TO-92)	SC-43	TA123E	PDTC123ES
PDTA123ET	SOT23	–	*21 <sup>(1)</sup>	PDTC123ET
PDTA123EU	SOT323	SC-70	*42 <sup>(1)</sup>	PDTC123EU

### Note

1. \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.  
\* = W: Made in China.

PNP resistor-equipped transistors;  
 R1 = 2.2 kΩ, R2 = 2.2 kΩ

PDTA123E series

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA123ES	<p style="text-align: center;"><i>MAM338</i></p>	1 2 3	base collector emitter
PDTA123EE PDTA123EEF PDTA123EK PDTA123ET PDTA123EU	<p style="text-align: center;">Top view <i>MDB271</i></p>	1 2 3	base emitter collector
PDTA123EM	<p style="text-align: center;">Bottom view <i>MDB267</i></p>	1 2 3	base emitter collector

PNP resistor-equipped transistors;  
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PDTA123E series

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTA123EE	–	plastic surface mounted package; 3 leads	SOT416
PDTA123EEF	–	plastic surface mounted package; 3 leads	SOT490
PDTA123EK	–	plastic surface mounted package; 3 leads	SOT346
PDTA123EM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm	SOT883
PDTA123ES	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA123ET	–	plastic surface mounted package; 3 leads	SOT23
PDTA123EU	–	plastic surface mounted package; 3 leads	SOT323

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CB0</sub>	collector-base voltage	open emitter	–	–50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	–50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	–10	V
V <sub>I</sub>	input voltage				
	positive		–	+10	V
	negative		–	–12	V
I <sub>O</sub>	output current (DC)		–	–100	mA
I <sub>CM</sub>	peak collector current		–	–100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
SOT883	notes 2 and 3	–	250	mW	
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

## Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60  $\mu$ m copper strip line.

PNP resistor-equipped transistors;  
R1 = 2.2 k $\Omega$ , R2 = 2.2 k $\Omega$

PDTA123E series

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	T <sub>amb</sub> ≤ 25 °C		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	830	K/W
	SOT490	notes 1 and 2	500	K/W
SOT883	notes 2 and 3	500	K/W	

### Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60  $\mu$ m copper strip line.

### CHARACTERISTICS

T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -50 V; I <sub>E</sub> = 0 A	-	-	-100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A	-	-	-1	$\mu$ A
		V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-50	$\mu$ A
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A	-	-	-2	mA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -20 mA	30	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -10 mA; I <sub>B</sub> = -0.5 mA	-	-	-150	mV
V <sub>i(off)</sub>	input-off voltage	I <sub>C</sub> = -1 mA; V <sub>CE</sub> = -5 V	-	-1.2	-0.5	V
V <sub>i(on)</sub>	input-on voltage	I <sub>C</sub> = -20 mA; V <sub>CE</sub> = -0.3 V	-2	-1.6	-	V
R1	input resistor		1.54	2.2	2.86	k $\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = i <sub>e</sub> = 0 A; V <sub>CB</sub> = -10 V; f = 1 MHz	-	-	3	pF

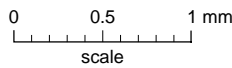
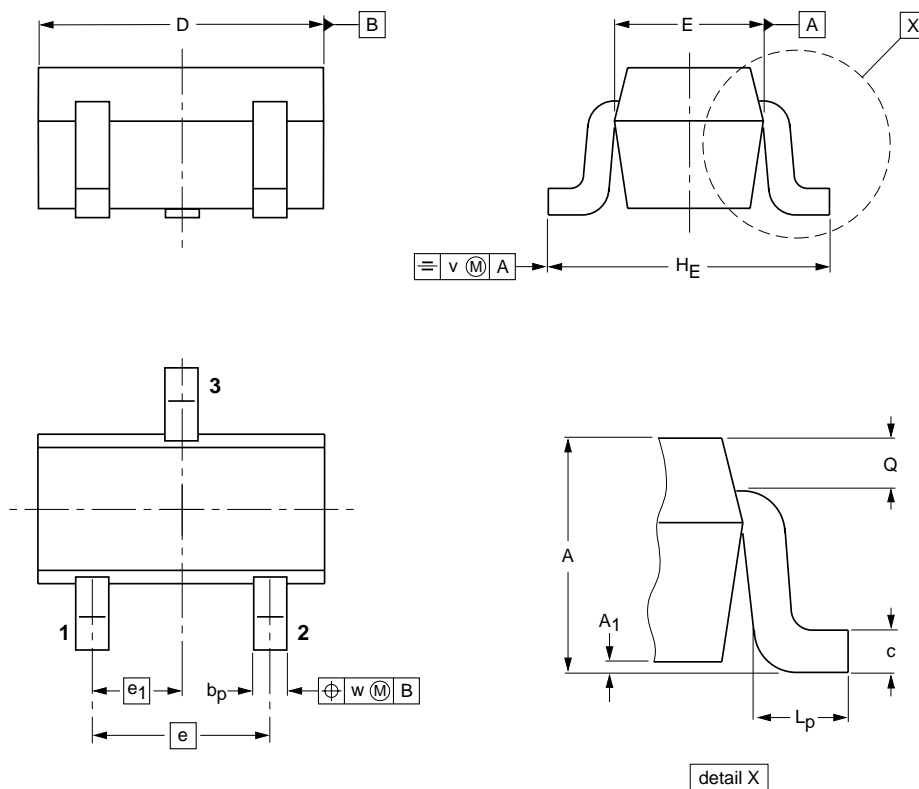
PNP resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

PDTA123E series

PACKAGE OUTLINES

Plastic surface-mounted package; 3 leads

SOT416



DIMENSIONS (mm are the original dimensions)

UNIT	A	A1 max	bp	c	D	E	e	e1	HE	Lp	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

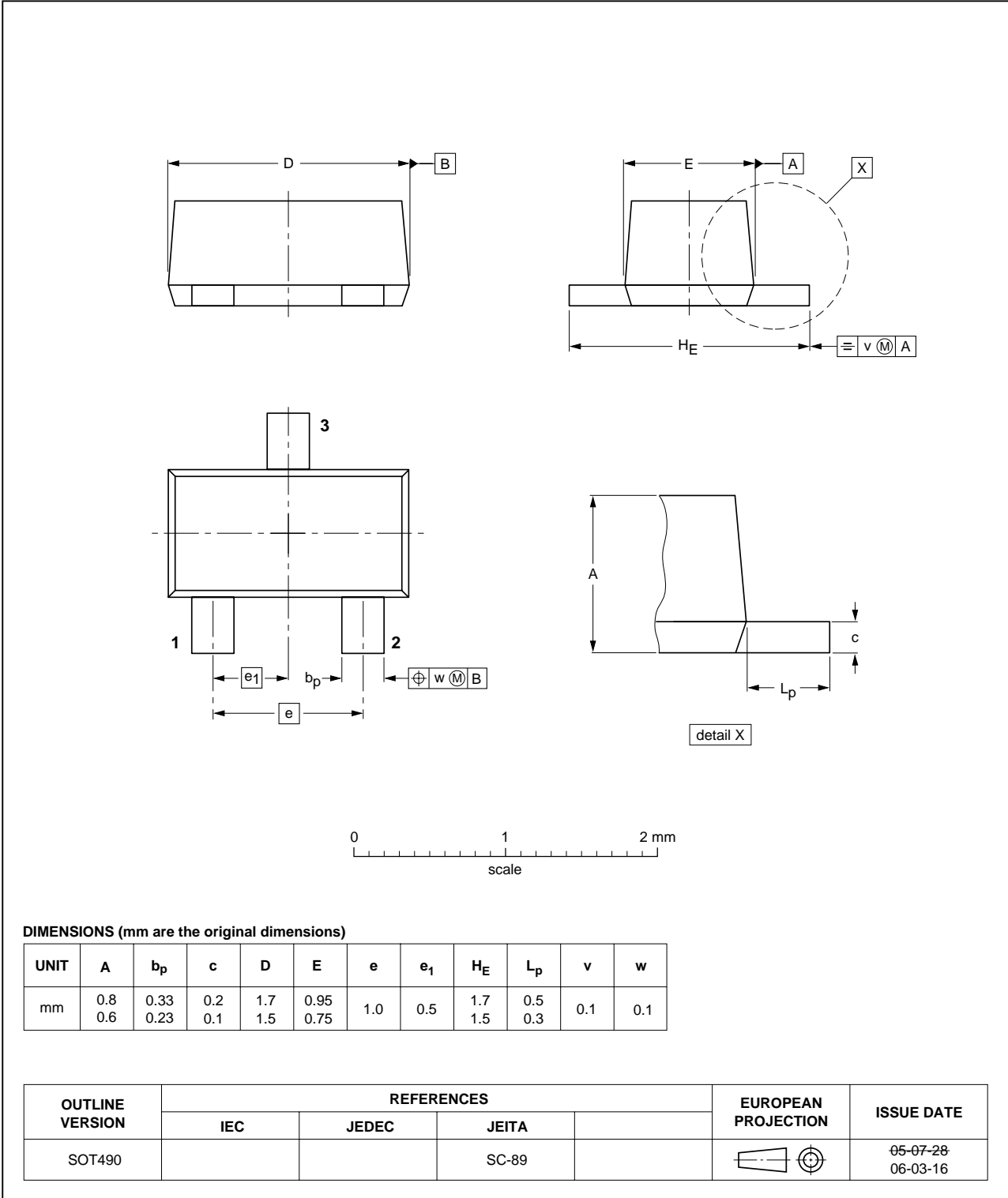
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT416			SC-75		04-11-04 06-03-16

PNP resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

PDTA123E series

Plastic surface-mounted package; 3 leads

SOT490



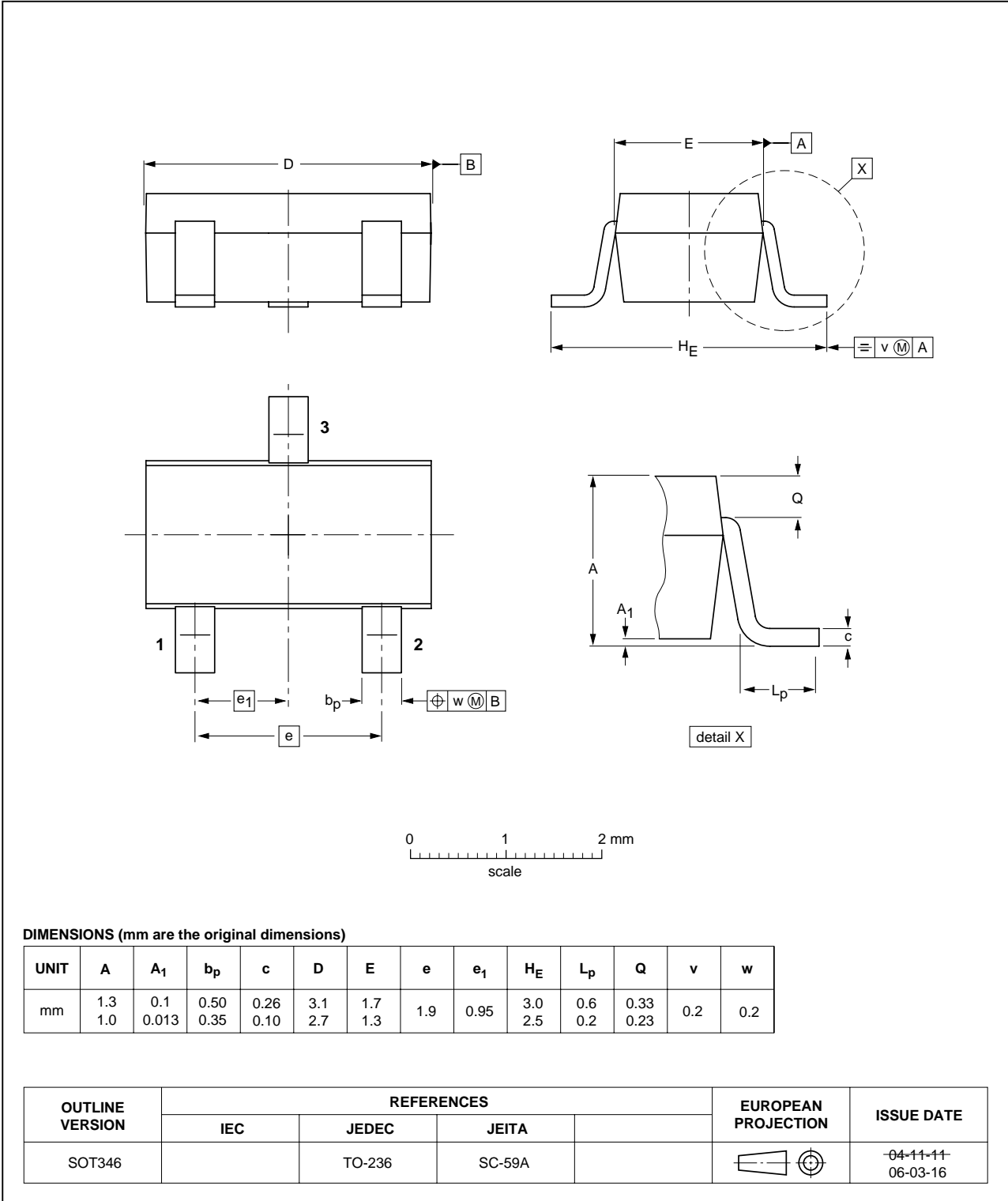


PNP resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

PDTA123E series

Plastic surface-mounted package; 3 leads

SOT346

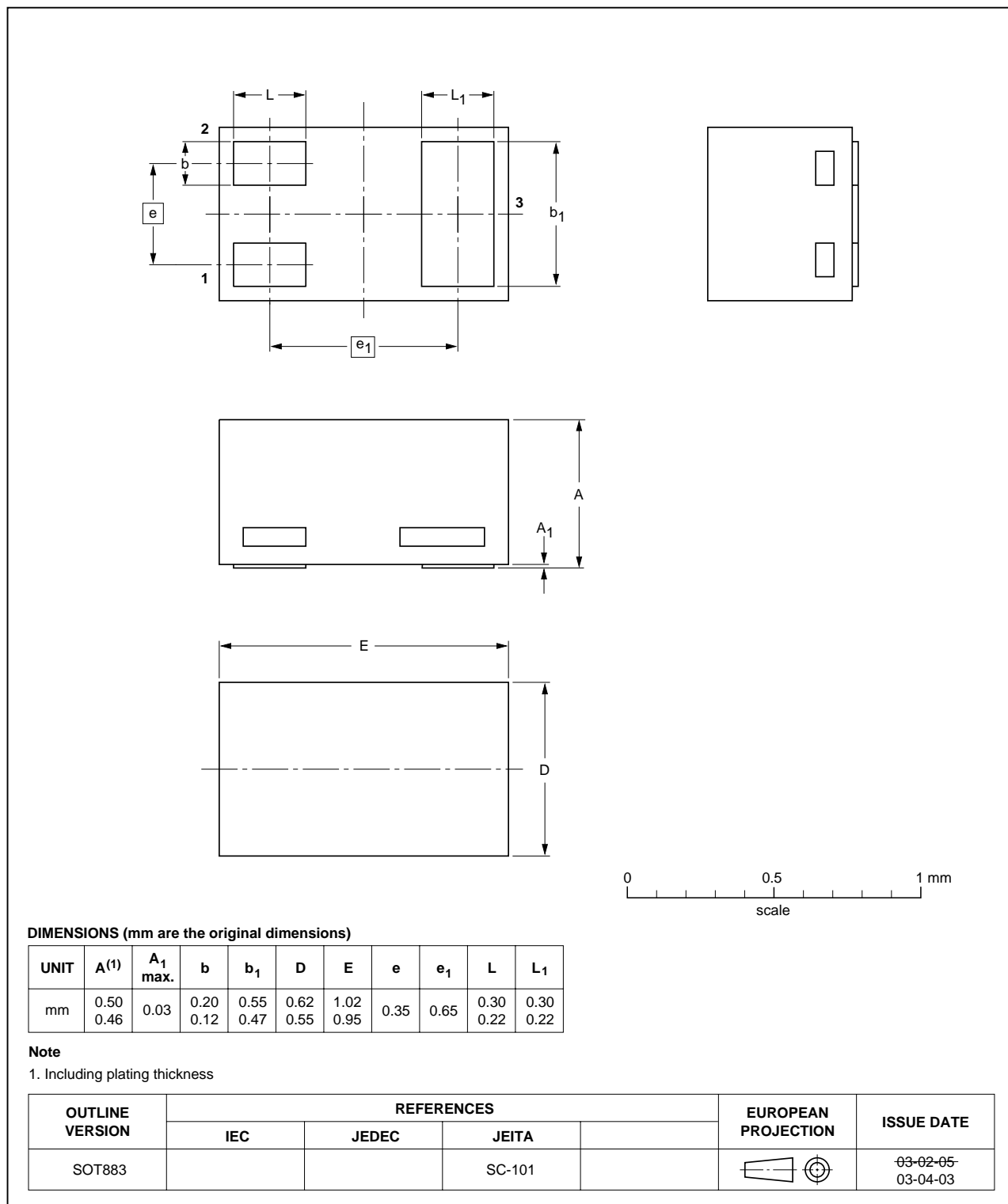


PNP resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

PDTA123E series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883

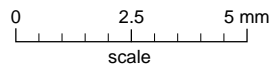
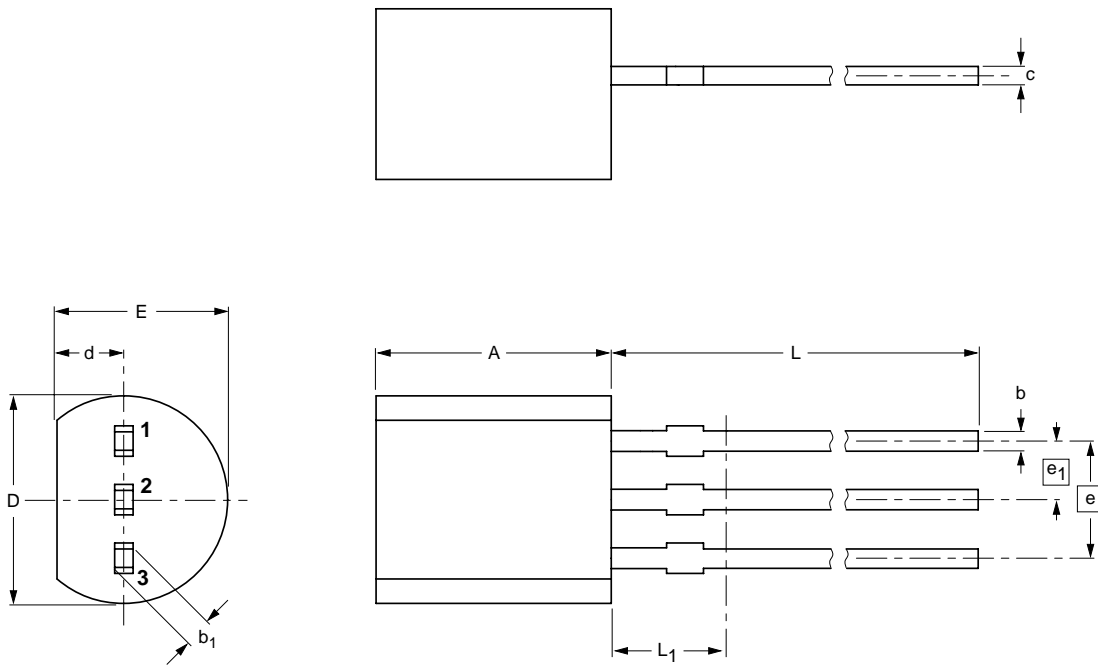


PNP resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

PDTA123E series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

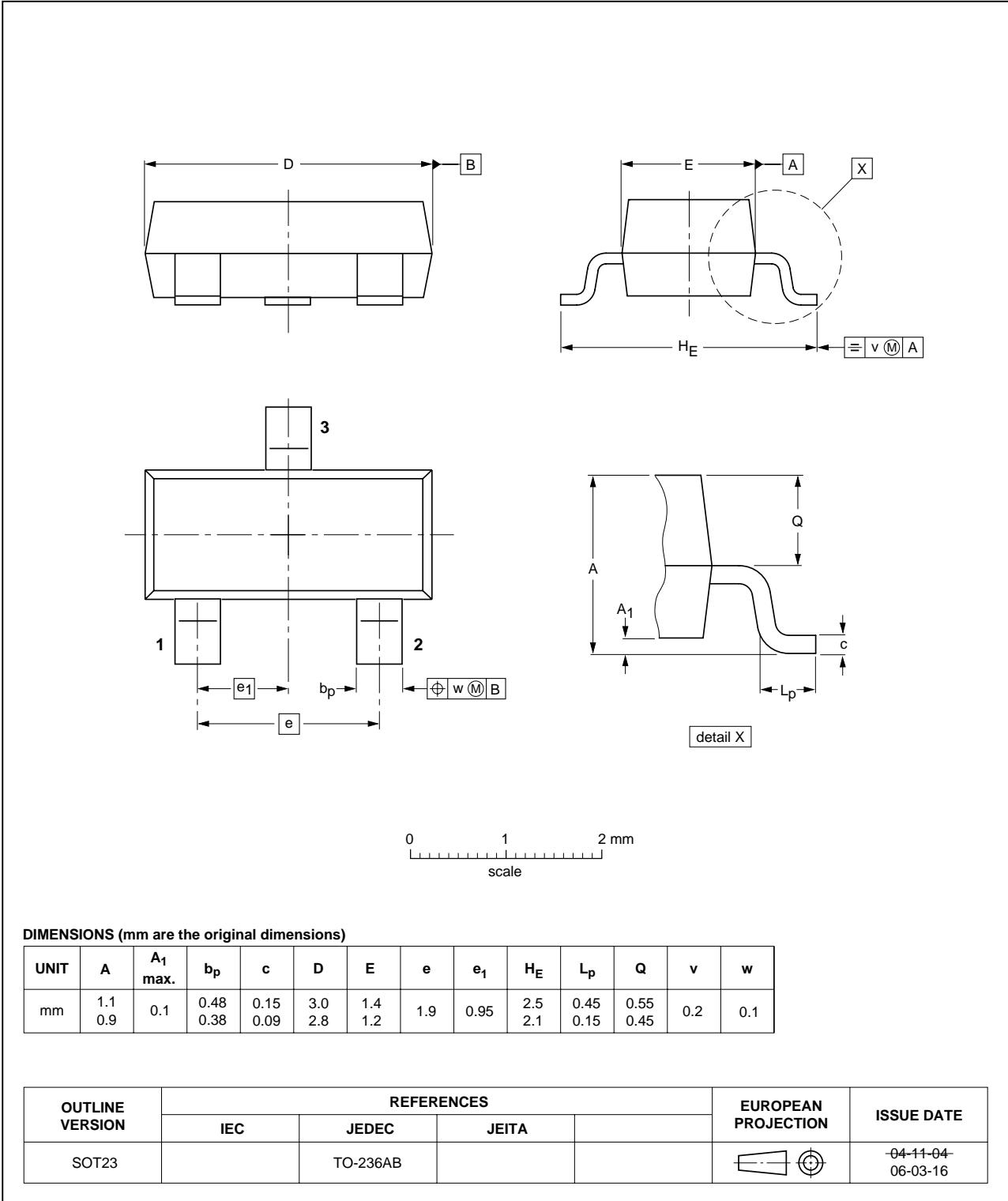
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		04-06-28 04-11-16

PNP resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

PDTA123E series

Plastic surface-mounted package; 3 leads

SOT23

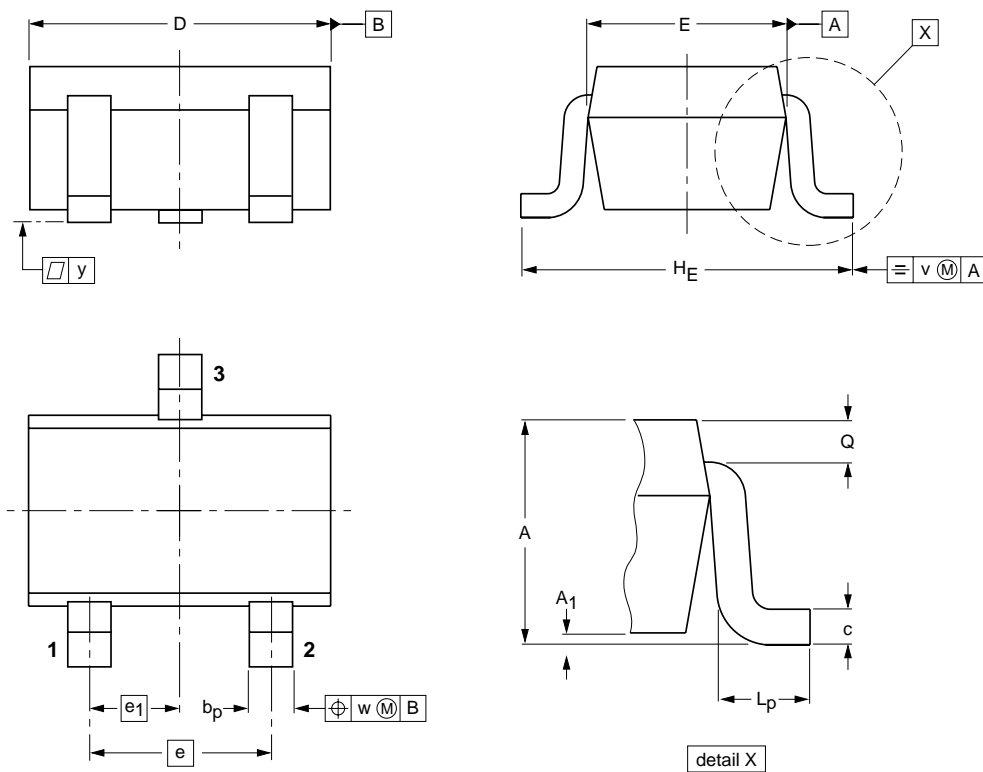


PNP resistor-equipped transistors;  
R1 = 2.2 kΩ, R2 = 2.2 kΩ

PDTA123E series

Plastic surface-mounted package; 3 leads

SOT323



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			<del>04-11-04</del> 06-03-16

PNP resistor-equipped transistors;  
R1 = 2.2 k $\Omega$ , R2 = 2.2 k $\Omega$

PDTA123E series

#### DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

#### Notes

1. Please consult the most recently issued document before initiating or completing a design.
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# ***NXP Semiconductors***

## **Customer notification**

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

## **Contact information**

For additional information please visit: <http://www.nxp.com>

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